

**SYSTEM AND METHOD FOR QUICK SELF-REFRESH EXIT WITH
TRANSITIONAL REFRESH**

THIS APPLICATION IS A CONTINUATION (CON.) OF U.S. PAT. 6,693,837, FILED APRIL 23 2002.
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5 The present invention is directed to dynamic random access memory ("DRAM") devices. More particularly, the present invention is directed to a system and method allowing DRAM devices to more efficiently exit from a self-refresh state so that the DRAM device can resume processing valid commands more quickly.

10 **BACKGROUND OF THE INVENTION**

Most computers and other digital systems have a system memory which often consists of dynamic random access memory ("DRAM") devices. DRAM devices are fairly inexpensive because a DRAM memory cell needs relatively few components to store a data bit as compared with other types of memory cells. Generally a DRAM memory cell
15 consists of a transistor/capacitor pair whereas, in a static random access device (SRAM), each memory cell comprises four or more transistors. Thus, DRAM memory cells have fewer components than SRAM memory cells. As a result, DRAM arrays occupy far less area on a semiconductor substrate compared to SRAM arrays of the same size. Thus, DRAM devices are far less expensive to produce than SRAM devices. A large system
20 memory can be implemented using DRAM devices for relatively low cost, making DRAM devices a very popular choice in many devices requiring a large memory capacity.

On the other hand, while DRAM devices are less expensive to produce than SRAM devices, DRAM devices suffer from the disadvantage that their memory cells must be continually refreshed because of the inherently transitory nature of their storage
25 technology. Over time, the voltage stored across the capacitor dissipates as a result of current leakage. To offset this problem, each memory cell regularly must be refreshed within a maximum refresh interval by determining whether a high or low voltage was stored across that capacitor, and recharging the capacitor to that voltage. The refresh process, which basically involves reading a memory cell through a sense amplifier to